REMARKS

The drawings stand objected to for being of poor quality and difficult to discern. Replacement drawings have been submitted in order to overcome the objection. Therefore, reconsideration and withdrawal of the objection is respectfully requested.

Examiner has objected to claim 1, instructing Applicants to insert a semicolon after "blocks" in claim 1 at line 4. Claim 1 has been amended accordingly. Therefore, reconsideration and withdrawal of the objection is respectfully requested.

Claims 1-39 are presently pending in the above-identified patent application. No claim is allowed.

Claims 1-39 are rejected pursuant to either 35 U.S.C. §102 as anticipated by the disclosure in Tavana et al. or pursuant to 35 U.S.C. §103 as obvious over the disclosure in Tavana et al. Thus each rejection relies on the disclosure in Tavana et al.

The Examiner is thanked for responding to the request made by the undersigned and providing information concerning the portions of the Tavara et al. reference relied upon in making the rejections. It is respectfully asserted that the portions of the reference relied upon by the Examiner do not teach or suggest what the Examiner relies upon for the claim rejections, but rather support applicants' position herein.

As previously noted in the response to the previous Office Action, independent claims 1 and 21 recite "mask programmed dedicated interface tracks connected

between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion." The remainder of the claims that are presently pending in the above-identified patent application depend, either directly or indirectly, from either claim 1 or from claim 21.

Tavana et al. disclose that the mask-defined routing 18 connects only the ASLA 14 to the programmable routing in switch matrices 26. The switch matrices 26 must further be programmed to connect elements in the ASLA 14 to any element in a CLB through switch matrices 26.

In paragraph 65 of the Office Action, the Examiner has relied on FIG. 6 of Tavana et al. According to the Examiner, "the switch matrices (326) provide interconnection between the CLBs (#22) (configurable logic blocks) that comprise the FPGA (col. 5, ll 32-54). Figure 6 discloses special mask-defined lines (#61, #62) that extend across the FPGA and connect to the local interconnect lines of the FPGA (FIG. 7, #s 63-66) that connect to the CLB blocks." It is respectfully submitted that this statement by the Examiner is an admission by the Examiner of one crucial difference between the prior-art disclosure of Tavana et al. and the invention as presently claimed.

As admitted by the Examiner, in the architecture disclosed in the Tavana et al. reference, the long lines 61 and 62 are connected at one end (right-hand side of FIG. 6) to the mask programmable routing 18 and at the other end to conductors associated with the switch matrices 26 (the matrix at the top left and the matrix at the center left in FIG. 6). This connection is *not* a connection to one of the "logic blocks" as recited in claim 1, or "modules or blocks" as recited in claim 21, since a further *programmable*

connection must be made between one of the switch matrices 26 and a CLB to which the switch matrices are *programmably connectable*. This difference is clearly shown in FIG. 6. Tavana et al clearly show that a CLB 22 (the equivalent of a "logic block" in the claims) is something different from a switch matrix 26. This difference is also clearly shown in FIG. 6. Therefore, the long lines 61 and 62 in Tavana et al. are *not* mask-programmably connected to the logic blocks as required by claims 1 and 21, since further programming of elements in a switch matrix must be performed to make a *programmable* connection between one of long lines 61 and 62 and a CLB. At best, the Tavana et al. reference shows mask programmable dedicated interconnect conductors connected between the ASLA 14 and the programmable switch matrices 26.

FIG. 7 of Tavana et al. does not add anything further, but simply shows part of FIG. 6 in more detail. Conductors 64, 65, and 66 are simply individual conductors associated with the switch matrices 26 and are not direct connections to logic elements in CLBs 22 (the "logic blocks of claims 1 and 21). Again, further *programmable* connections must be made to make final connections to the logic elements in CLBs 22.

Accordingly, the Tavana et al. reference does not disclose or suggest the limitations of claims 1 and 21 "mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion" in claim 1 and "mask programmed dedicated interface tracks connected between said modules or blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion" in claim 21. These limitations require that the mask-programmable conductors make direct connections

between the ASIC portion and the individual logic blocks in the FPGA portion. The Tavana et al. reference does not disclose such a feature in an FPGA architecture.

Applicants respectfully submit that claims 1 and 21 are patentable over the Tavana et al. reference. Since claims 2-20 and 22-39 depend from claims 1 and 21 respectively, they are also patentable as they contain the same limitations as their respective parent claims. Reconsideration and withdrawal of the rejection is respectfully requested.

If the Examiner has any questions regarding this application or this response, the Examiner is requested to telephone the undersigned at 775-586-9500.

Respectfully submitted,
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